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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,483	09/12/2003	Koji Mishima	2003_1305	6334
513	7590	12/15/2004	EXAMINER	
WENDEROTH, LIND & PONACK, L.L.P.			LEADER, WILLIAM T	
2033 K STREET N. W.			ART UNIT	
SUITE 800			PAPER NUMBER	
WASHINGTON, DC 20006-1021			1742	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/660,483	<b>Applicant(s)</b> MISHIMA ET AL	
	<b>Examiner</b> William T. Leader	<b>Art Unit</b> 1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/492,138.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>9/12/03</u> . | 6) <input type="checkbox"/> Other: ____.  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 4, 5 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Dubin et al (5,972,192).

3. The Dubin et al patent is directed to electroplating copper onto a semiconductor substrate with vias and trenches. In one embodiment disclosed by Dubin et al, the plating may be conducted in separate phases. Initially the wafer is brought into contact with a copper electroplating solution containing a leveling agent. During the first phase an electric current is applied to electroplate copper to

a thickness of about one half of the width of the opening of the trench or via. The electroplating is stopped and an anodic electric current, opposite to the cathodic current used during the first plating phase, is applied to electro-etch the deposit. The etching step is carried out to reduce the thickness of the deposited copper to have about the same or smaller thickness at the corners of openings than on the side walls. In the third phase, cathodic current is again applied to deposit the desired amount of copper. See column 7, lines 1-15. Thus, all steps recited in instant claim 1 are taught by Dubin et al. With respect to the limitations of claims 5 and 6, all plating and etching phases are performed with the plating solution.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor

and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin et al.

7. Claim 2 differs from the process disclosed by Dubin et al by reciting the current density of the electric current used during the etching step, while claim 3 differs by reciting the period of time during which the etching step is carried out. Dubin et al is silent as to the current density and duration of the electro-etching phase of the three-phase embodiment. However, Dubin et al does disclose that in the single-phase embodiment illustrated in example 1, the cathodic electric current applied to deposit copper was in the range of about 5-50 mA/cm<sup>2</sup>. Plating results were observed after 20, 40 and 80 seconds. These ranges use values of current density and duration overlapping the ranges recited by applicant. The current density and duration of treatment are result-effective parameters. Choice of appropriate values of these parameters to obtain the results disclosed by Dubin et al would have been within the skill of one of ordinary skill in the art.

8. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reid et al (6,716,334) in view of Landau (6,261,433).

9. The Reid et al patent is directed to a method and apparatus for electroplating a metal onto a semiconductor wafer. The plating metal may be copper (column 2, lines 51-54). Reid et al teach that in conventional plating, the wafer is processed serially through three separate stages: pre-treatment, plating and rinsing (column 1, lines 11-15). Reid et al disclose an apparatus in which multiple operations may be performed. These operations include spraying pure water onto the wafer. Reid et al recognize that it is undesirable for excess water to enter the plating solution because the solution would be diluted (column 1, lines 29-34). The apparatus of Reid et al is designed so that the wafer may be spun while water is sprayed onto the wafer. During the spraying, the wafer may be positioned so that the water spun from the wafer is collected separately and does not dilute the plating bath (column 3, lines 32-60).

10. Instant claim 7 differs from the process of Reid et al by reciting bringing the substrate into contact with a processing liquid offering increased wettability between the plating solution and the substrate surface. As noted above, Reid et al discloses pretreatment prior to plating, but does not describe the pretreatment in detail.


11. The Landau patent is directed to electroplating a metal onto semiconductor wafers. Landau teaches that prior to plating, ultra pure water can be introduced to the substrate plating surface to ensure complete wetting which enhances the electroplating process (column 18, lines 35-39). Landau also notes that surfactants improve wetting by reducing surface tension (column 18, lines 40-41). It would have been obvious to have utilized the wetting treatment disclosed by Landau as the pretreatment in the process of Reid et al because complete wetting of the substrate plating surface with the plating solution would have been obtained. By teaching that dilution of the plating solution should be avoided, Reid et al suggest the removal of excess wetting liquid from the substrate surface after pretreatment and prior to plating. As noted above, Reid et al teaches removing liquid from the wafer by spinning the wafer. This meets the limitation of instant claim 8. The apparatus of Reid et al is adapted to performing multiple process steps, meeting the limitation of instant claim 9.

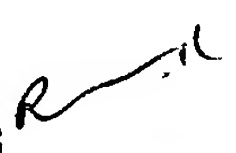
Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 571-272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.



If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
William Leader  
December 3, 2004

  
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SUPERVISORY PATENT EXAMINER  
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